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AMENDMENTS TO THE SPECIFICATION:

On page 11, line 18, please amend the paragraph as follows:

The input voltage of 2.5V charges the lower capacitor C_{p1a} to 2.5V through transistor P_{1a} which is turned on. The upper capacitor C_{p1b} is charged with 2.5V across it and presents 7.5V to the output. Charge is pumped to the output through transistor P_{1b} to maintain the output at this voltage.

On page 12, line 15, please amend the paragraph as follows:

FIG. 5 shows an integrated circuit device 30 including an active matrix liquid crystal display device which uses a TFT switching array 32. The switching array and a charge pump circuit 34 are provided on a common substrate 36, and a low voltage power supply 38 (for example a 3V battery) provides power to the integrated circuit 30 36.

On page 12, line 15, please insert the following new paragraph:

At the outputs V_{out1} and V_{out2} , capacitors C_1 and C_2 are provided and connected to ground. Resistors R_{11} and R_{12} are provided.

On page 13, line 11, please insert the following new paragraph:

At the outputs V_{out1} and V_{out2} , capacitors C_1 and C_2 are provided and connected to ground. Resistors R_{11} and R_{12} are provided.

On page 14, line 7, please amend the paragraph as follows:

FIG. 9 shows a possible circuit for implementing the schematic configuration shown in FIG. 8. Transistor N1b and capacitor Cbs1a in conjunction with control signal ϕ_a generate level shifted voltage signals for switching the charge pump transistor N1a. Transistor N1c and capacitor Cbs1b in conjunction with control signal ϕ_b generate voltage signals for switching the charge pump transistor P1. Transistor P2b and capacitor Cbs2a in conjunction with control signal ϕ_a generate voltage signals for switching the charge pump transistor P2a. Transistor P2c and capacitor Cbs2b in conjunction with control signal ϕ_b generate voltage signals for switching the charge pump transistor N2. This circuit requires the generation of 6 control signal ϕ , ϕ_a , ϕ_b and their complements.

On page 14, line 18, please insert the following new paragraph:

At the outputs V_{out1} and V_{out2} , capacitors C_1 and C_2 are provided and connected to ground. Resistors R_{11} and R_{12} are provided.

On page 15, line 10, please insert the following new paragraph:

At the outputs V_{out1} and V_{out2} , capacitors C_1 and C_2 are provided and connected to ground.
Resistors R_{11} and R_{12} are provided.